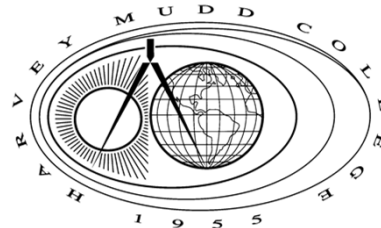


Introduction to CMOS VLSI Design

Lecture 18: Design for Low Power

David Harris



Harvey Mudd College

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Outline

- Power and Energy
- Dynamic Power
- Static Power
- Low Power Design

Power and Energy

- ❑ Power is drawn from a voltage source attached to the V_{DD} pin(s) of a chip.

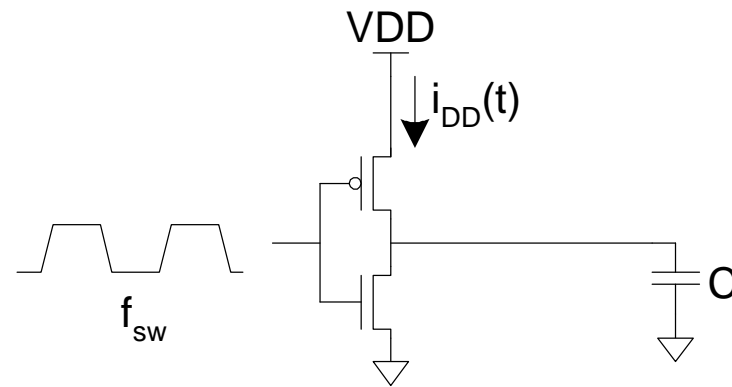
- ❑ Instantaneous Power: $P(t) = i_{DD}(t)V_{DD}$

- ❑ Energy:
$$E = \int_0^T P(t)dt = \int_0^T i_{DD}(t)V_{DD}dt$$

- ❑ Average Power:
$$P_{\text{avg}} = \frac{E}{T} = \frac{1}{T} \int_0^T i_{DD}(t)V_{DD}dt$$

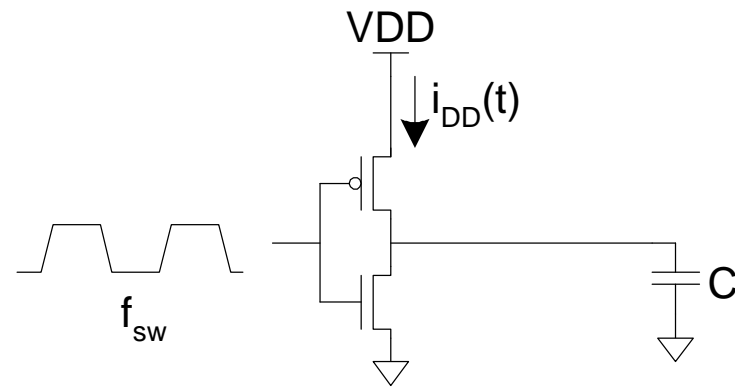
Dynamic Power

- ❑ Dynamic power is required to charge and discharge load capacitances when transistors switch.
- ❑ One cycle involves a rising and falling output.
- ❑ On rising output, charge $Q = CV_{DD}$ is required
- ❑ On falling output, charge is dumped to GND
- ❑ This repeats Tf_{sw} times over an interval of T



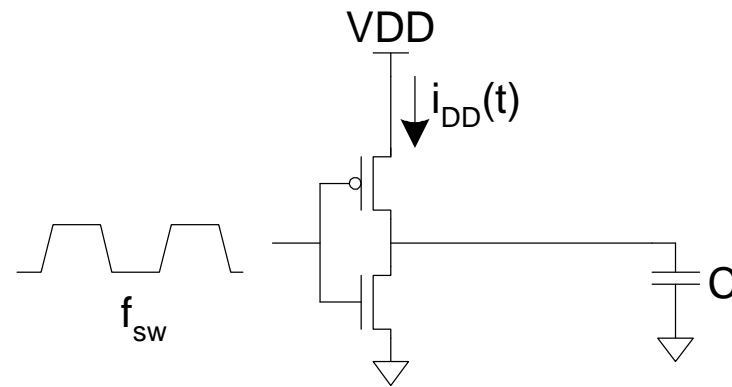
Dynamic Power Cont.

$$P_{\text{dynamic}} =$$



Dynamic Power Cont.

$$\begin{aligned} P_{\text{dynamic}} &= \frac{1}{T} \int_0^T i_{DD}(t) V_{DD} dt \\ &= \frac{V_{DD}}{T} \int_0^T i_{DD}(t) dt \\ &= \frac{V_{DD}}{T} [T f_{\text{sw}} C V_{DD}] \\ &= C V_{DD}^2 f_{\text{sw}} \end{aligned}$$



Activity Factor

- ❑ Suppose the system clock frequency = f
- ❑ Let $f_{sw} = \alpha f$, where α = activity factor
 - If the signal is a clock, $\alpha = 1$
 - If the signal switches once per cycle, $\alpha = \frac{1}{2}$
 - Dynamic gates:
 - Switch either 0 or 2 times per cycle, $\alpha = \frac{1}{2}$
 - Static gates:
 - Depends on design, but typically $\alpha = 0.1$

❑ Dynamic power:
$$P_{\text{dynamic}} = \alpha C V_{DD}^2 f$$

Short Circuit Current

- ❑ When transistors switch, both nMOS and pMOS networks may be momentarily ON at once
- ❑ Leads to a blip of “short circuit” current.
- ❑ $< 10\%$ of dynamic power if rise/fall times are comparable for input and output

Example

- 200 Mtransistor chip
 - 20M logic transistors
 - Average width: 12λ
 - 180M memory transistors
 - Average width: 4λ
 - 1.2 V 100 nm process
 - $C_g = 2 \text{ fF}/\mu\text{m}$

Dynamic Example

- ❑ Static CMOS logic gates: activity factor = 0.1
- ❑ Memory arrays: activity factor = 0.05 (many banks!)

- ❑ Estimate dynamic power consumption per MHz.
Neglect wire capacitance and short-circuit current.

Dynamic Example

- ❑ Static CMOS logic gates: activity factor = 0.1
- ❑ Memory arrays: activity factor = 0.05 (many banks!)
- ❑ Estimate dynamic power consumption per MHz.
Neglect wire capacitance.

$$C_{\text{logic}} = (20 \times 10^6)(12\lambda)(0.05 \mu\text{m} / \lambda)(2 \text{ fF} / \mu\text{m}) = 24 \text{ nF}$$

$$C_{\text{mem}} = (180 \times 10^6)(4\lambda)(0.05 \mu\text{m} / \lambda)(2 \text{ fF} / \mu\text{m}) = 72 \text{ nF}$$

$$P_{\text{dynamic}} = [0.1C_{\text{logic}} + 0.05C_{\text{mem}}](1.2)^2 f = 8.6 \text{ mW/MHz}$$

Static Power

- ❑ Static power is consumed even when chip is quiescent.
 - Ratioed circuits burn power in fight between ON transistors
 - Leakage draws power from nominally OFF devices

$$I_{ds} = I_{ds0} e^{\frac{V_{gs} - V_t}{nV_T}} \left[1 - e^{\frac{-V_{ds}}{V_T}} \right]$$

$$V_t = V_{t0} - \eta V_{ds} + \gamma \left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s} \right)$$

Ratio Example

- ❑ The chip contains a 32 word x 48 bit ROM
 - Uses pseudo-nMOS decoder and bitline pullups
 - On average, one wordline and 24 bitlines are high
- ❑ Find static power drawn by the ROM
 - $\beta = 75 \mu\text{A}/\text{V}^2$
 - $V_{tp} = -0.4\text{V}$

Ratio Example

- ❑ The chip contains a 32 word x 48 bit ROM
 - Uses pseudo-nMOS decoder and bitline pullups
 - On average, one wordline and 24 bitlines are high
- ❑ Find static power drawn by the ROM

- $\beta = 75 \mu\text{A}/\text{V}^2$

- $V_{tp} = -0.4\text{V}$

- ❑ Solution:

$$I_{\text{pull-up}} = \beta \frac{(V_{DD} - |V_{tp}|)^2}{2} = 24\mu\text{A}$$

$$P_{\text{pull-up}} = V_{DD} I_{\text{pull-up}} = 29\mu\text{W}$$

$$P_{\text{static}} = (31 + 24)P_{\text{pull-up}} = 1.6 \text{ mW}$$

Leakage Example

- ❑ The process has two threshold voltages and two oxide thicknesses.
- ❑ Subthreshold leakage:
 - 20 nA/ μm for low V_t
 - 0.02 nA/ μm for high V_t
- ❑ Gate leakage:
 - 3 nA/ μm for thin oxide
 - 0.002 nA/ μm for thick oxide
- ❑ Memories use low-leakage transistors everywhere
- ❑ Gates use low-leakage transistors on 80% of logic

Leakage Example Cont.

- Estimate static power:

Leakage Example Cont.

□ Estimate static power:

– High leakage: $(20 \times 10^6)(0.2)(12\lambda)(0.05\mu m / \lambda) = 2.4 \times 10^6 \mu m$

– Low leakage: $(20 \times 10^6)(0.8)(12\lambda)(0.05\mu m / \lambda) +$
 $(180 \times 10^6)(4\lambda)(0.05\mu m / \lambda) = 45.6 \times 10^6 \mu m$

$$I_{static} = (2.4 \times 10^6 \mu m) \left[(20nA / \mu m) / 2 + (3nA / \mu m) \right] +$$
$$(45.6 \times 10^6 \mu m) \left[(0.02nA / \mu m) / 2 + (0.002nA / \mu m) \right]$$
$$= 32mA$$

$$P_{static} = I_{static} V_{DD} = 38mW$$

Leakage Example Cont.

□ Estimate static power:

– High leakage: $(20 \times 10^6)(0.2)(12\lambda)(0.05\mu m / \lambda) = 2.4 \times 10^6 \mu m$

– Low leakage: $(20 \times 10^6)(0.8)(12\lambda)(0.05\mu m / \lambda) +$
 $(180 \times 10^6)(4\lambda)(0.05\mu m / \lambda) = 45.6 \times 10^6 \mu m$

$$I_{static} = (2.4 \times 10^6 \mu m) \left[(20nA / \mu m) / 2 + (3nA / \mu m) \right] +$$
$$(45.6 \times 10^6 \mu m) \left[(0.02nA / \mu m) / 2 + (0.002nA / \mu m) \right]$$
$$= 32mA$$

$$P_{static} = I_{static} V_{DD} = 38mW$$

□ If no low leakage devices, $P_{static} = 749 mW$ (!)

Low Power Design

- ❑ Reduce dynamic power
 - α :
 - C:
 - V_{DD} :
 - f:
- ❑ Reduce static power

Low Power Design

- ❑ Reduce dynamic power
 - α : clock gating, sleep mode
 - C:
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Low Power Design

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 - C : small transistors (esp. on clock), short wires
 - V_{DD} :
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- ❑ Reduce static power

Low Power Design

- ❑ Reduce dynamic power
 - α : clock gating, sleep mode
 - C: small transistors (esp. on clock), short wires
 - V_{DD} : lowest suitable voltage
 - f:
- ❑ Reduce static power

Low Power Design

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 - α : clock gating, sleep mode
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Low Power Design

- ❑ Reduce dynamic power
 - α : clock gating, sleep mode
 - C: small transistors (esp. on clock), short wires
 - V_{DD} : lowest suitable voltage
 - f: lowest suitable frequency
- ❑ Reduce static power
 - Selectively use ratioed circuits
 - Selectively use low V_t devices
 - Leakage reduction:
stacked devices, body bias, low temperature